A Self-Consistent Method for Complete Small-Signal Parameter Extraction of InP-Based Heterojunction Bipolar Transistors (HBT's)

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***Abstract*— A complete method for parameter extraction from small-signal measurements of InP-based heterojunction bipolar transistors (HBT's) is presented. Employing analytically derived equations, a numerical solution is sought for the best fit between the model and the measured data. Through parasitics extraction and an optimization process, a realistic model for a self-aligned HBT technology is obtained. The results of the generated s-parameters from the model for a 2×10 μm^2 emitter area device are presented over a frequency range of 250 MHz–36 GHz with excellent agreement to the measured data.**

I. Introduction

THE HIGH-SPEED potential of heterojunction bipolar transistors (HBT's) in InP-based systems makes them promising candidates for optoelectronic applications [1], [2]. The advantages of HBT's in high-speed applications result from two features: their structure and their superior carrier transport properties. In order to optimize the performance of our HBT-based photoreceiver optoelectronic integrated circuit (OEIC) [1], a complete and accurate equivalent circuit model for the transistor is needed. To evaluate these equivalent circuit device parameters, we can rely on optimization techniques or try to measure them. Although numerical optimization is often used to fit the model-generated S-parameters to the measured S-parameters, the resulting device element values depend on the starting values and are not unique. On the other hand, the measurement of too many parameters is time consuming or, sometimes, impossible. Many research groups have reported attempts to balance between how many parameters can be extracted from multiple types of measurements and how many must be obtained from optimization [3]–[8].

One important issue in the different approaches is the system chosen to be studied, usually the AlGaAs/GaAs system [3]–[7]. Due to its characteristics, this material system allows important approximations to the equivalent circuit model, and the optimization step can even be avoided. But for the InP-based HBT technology, parameters like high intrinsic base resistance, high base-collector junction resistance, and relatively small extrinsic base–collector junction capacitance prohibit us to utilize some important approximations present in [5]–[7]. In [8] the authors study an InP-based HBT also, but we cannot use their procedure of estimating from geometry the ratio between intrinsic and extrinsic components of base-collector junction capacitance because of the reduction of the extrinsic component by chemical etching in our devices [9]. We want to be able to evaluate the effectiveness of this process as well, so we addressed the problem with different steps.

So, our approach is a translation of the physically based T-model equivalent circuit for the individual device into analytical equations that will fit our measured S-parameter data. With these equations transformed to Z-parameters, we analyze the experimental data, extracting the maximum amount of information, parameter values, and constraints in order to minimize the number of unknown parameters that inevitably must be evaluated by a final numerical optimization process. This method is shown to be an appropriate technique to provide a realistic model for InP-based HBT technology without approximations or device geometry estimations that are specific to material system or transistor technology. To our knowledge, this is the first self-consistent method for transistors operating beyond 80 GHz. However, it relies on complementing small-signal S-parameters with dc measurements of collector and emitter resistances, minimizing, therefore, the number of total parameters for the final fitting.

II. Model Analysis

The HBT small signal equivalent circuit used for this work is the T-model shown in Fig. 1. In this model, l_b, l_e, and l_c represent the pad parasitic inductances, and $c_{\rm pbc}, c_{\rm pbe}$, and $c_{\rm pce}$, the pad parasitic capacitances. These parasitics will be obtained from measurements of test structures on the same wafer as the device under study. The pad parasitic resistances are assumed small and are incorporated into the HBT extrinsic contact resistances. The dashed box in Fig. 1 emphasizes the HBT device without the pad parasitics. For this layer of the T-model equivalent circuit, the Z-parameters equations become

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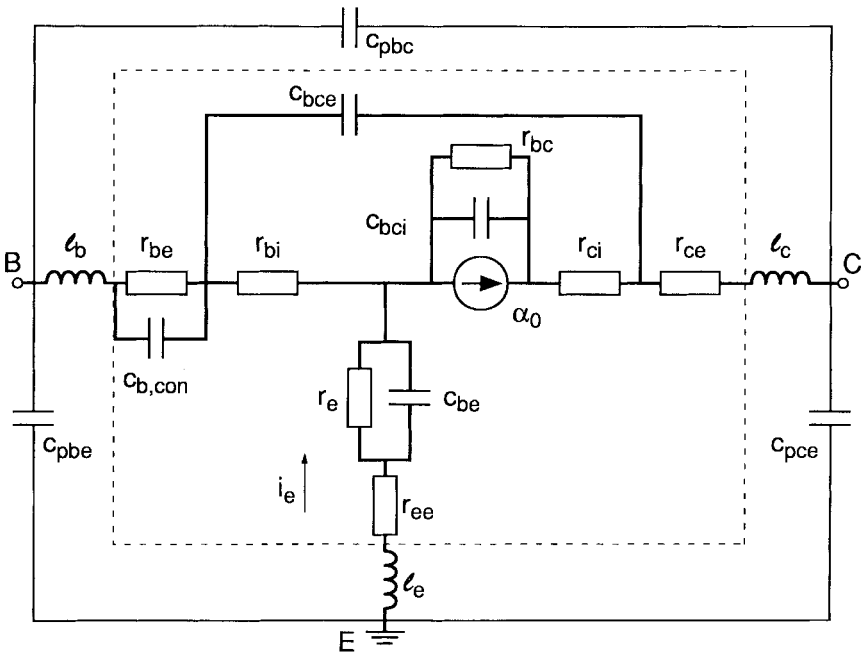

V_{CE}	1.8 V	ℓ_e	35 pH	c_{pce}	15 fF	c_{bci}	7 fF	α_0	0.995	r_{ee}	11.0 Ω
I_C	10 mA	ℓ_b	52 pH	c_{pbc}	5 fF	c_{bce}	22 fF	τ_i	0.66 ps	r_e	7.0 Ω
f_T	88 GHz	ℓ_c	55 pH	r_{be}	10.3 Ω	$c_{b,con}$	680 fF	r_{ce}	7 Ω	c_{be}	53 fF
f_{max}	63 GHz	c_{pbe}	13 fF	r_{bi}	70 Ω	r_{bc}	1 MΩ	r_{ci}	5 Ω		

Fig. 1. HBT small-signal T-model equivalent circuit. At the bottom of the figure, the bias conditions and characteristic frequencies for the InP-Based HBT are shown along with the equivalent circuit parameters obtained by measurement, parameter extraction, and/or optimization process.

(after a few matrix manipulations) the expressions

$$Z_{11}-Z_{12}=z_{\rm be}+\frac{r_{\rm bi}z_{\rm fb}}{r_{\rm bi}+r_{\rm ci}+z_{\rm bc}+z_{\rm fb}} \tag{1}$$

$$Z_{22}-Z_{21}=r_{\rm ce}+\frac{(r_{\rm ci}+z_{\rm bc})z_{\rm fb}}{r_{\rm bi}+r_{\rm ci}+z_{\rm bc}+z_{\rm fb}} \tag{2}$$

$$Z_{12}-Z_{21}=\frac{\alpha z_{\rm bc}z_{\rm fb}}{r_{\rm bi}+r_{\rm ci}+z_{\rm bc}+z_{\rm fb}} \tag{3}$$

$$Z_{12}=z_e+r_{\rm bi}\frac{(r_{\rm ci}+z_{\rm bc}(1-\alpha))}{r_{\rm bi}+r_{\rm ci}+z_{\rm bc}+z_{\rm fb}} \tag{4}$$

where

$$z_{\rm be}=\frac{r_{\rm be}}{1+(\omega r_{\rm be}c_{b,\rm con})^2}-j\frac{\omega r_{\rm be}^2c_{b,\rm con}}{1+(\omega r_{\rm be}c_{b,\rm con})^2}$$

$$z_e=r_{\rm ee}+\frac{r_e}{1+(\omega r_ec_{\rm be})^2}-j\frac{\omega r_e^2c_{\rm be}}{1+(\omega r_ec_{\rm be})^2}$$

$$z_{\rm bc}=\frac{r_{\rm bc}}{1+(\omega r_{\rm bc}c_{\rm bci})^2}-j\frac{\omega r_{\rm bc}^2c_{\rm bci}}{1+(\omega r_{\rm bc}c_{\rm bci})^2}$$

and

$$z_{\rm fb}=-j\frac{1}{\omega c_{\rm bce}}.$$

In a first approximation, we have assumed that the extrinsic collector, intrinsic collector, and intrinsic base impedances can be well represented at the frequency range of interest by pure resistances ($r_{\rm ce}, r_{\rm ci}$, and $r_{\rm bi}$, respectively) without any capacitive or inductive component.

We describe the current source by the dc-current gain α_0, the 3-dB roll-off frequency $\omega=1.2/\tau_B$, the base and collector transit times τ_B and τ_C, and the empirical factor $m=0.22$. The intrinsic transit time is defined as $\tau_i=((m+1)\tau_B/1.2)+(\tau_C/2)$, and the approximation below is valid because, for InGaAs/InP HBT's, $\omega\tau_i\ll 1$ [5], [10]

$$\alpha=\frac{1}{(1+j\omega r_ec_{\rm be})}\frac{\alpha_0e^{-j\omega[(m\tau_B/1.2)+(\tau_C/2)]}}{\left(1+j\frac{\omega}{\omega_\beta}\right)}\approx\frac{\alpha_0(1-j\omega\tau_i)}{(1+j\omega r_ec_{\rm be})}.$$

Expanding (1)–(3) and studying their frequency behavior, we arrive at the following expressions:

$$c_{\rm bct}\equiv\frac{-{\rm Im}[Z_{22}-Z_{21}]}{\omega}\approx c_{\rm bci}+c_{\rm bce} \tag{5}$$

$$r_{\rm bt}\equiv{\rm Re}[Z_{11}-Z_{12}]\approx r_{\rm be}+r_{\rm bi}\frac{c_{\rm bci}}{c_{\rm bci}+c_{\rm bce}} \tag{6}$$

$$r_{\rm ct}\equiv{\rm Re}[Z_{22}-Z_{21}]\approx r_{\rm ce}+\left(\frac{c_{\rm bci}}{c_{\rm bci}+c_{\rm bce}}\right)^2\left(r_{\rm ci}-r_{\rm bi}\frac{c_{\rm bce}}{c_{\rm bci}}+\frac{1}{\omega^2r_{\rm bc}c_{\rm bci}^2}\right). \tag{7}$$

Equations (5)–(7) incorporate the approximations $(\omega r_{\rm bc}c_{\rm bci})^2\gg 1$ and $[\omega(r_{\rm bi}+r_{\rm ci})c_{\rm bci}]^2\ll 1$. To be valid simultaneously, these approximations imply that $r_{\rm bi}, r_{\rm ci}\ll r_{\rm bc}$, which is typically the case in InGaAs/InP HBT's. In (6) it is also assumed that $(\omega r_{\rm be}c_{b,\rm con})^2\ll 1$.

These approximations will determine a frequency range over which (5) and (6) will have constant values. For our devices,

with appropriate technology parameter values, this frequency range spans from approximately 1 to 10 GHz.

In the case of (7), a constant value will be attained only at high frequencies. At low frequencies, this expression will approach the resistance value of the base–collector junction

$$\mathrm{Re}[Z_{22}-Z_{21}]_{\omega\to 0}\approx r_{\mathrm{bc}}. \tag{8}$$

We find also the following useful expressions:

$$\alpha_0 \approx \mathrm{Re}\frac{[Z_{12}-Z_{21}]}{[Z_{22}-Z_{21}]} \tag{9}$$

$$\begin{aligned}\tau_d &\cong \mathrm{PHA}\frac{[Z_{12}-Z_{21}]}{[Z_{22}-Z_{21}]}\\ &\approx \tau_i + r_e c_{\mathrm{be}} + r_{\mathrm{ci}} c_{\mathrm{bci}} + r_{\mathrm{ce}}(c_{\mathrm{bci}}+c_{\mathrm{bce}})\end{aligned} \tag{10}$$

$$\begin{aligned}r_{\mathrm{et}} &\equiv \mathrm{Re}[Z_{12}] \approx r_e + r_{\mathrm{ee}} + r_{\mathrm{bi}}(1-\alpha_0)\frac{c_{\mathrm{bce}}}{c_{\mathrm{bci}}+c_{\mathrm{bce}}}\\ &\equiv r_e + r_{\mathrm{ee}} + \delta.\end{aligned} \tag{11}$$

Equations (9) and (10) incorporate the approximations $(\omega r_{\mathrm{bc}} c_{\mathrm{bce}})^2 \gg 1$ and $[\omega(r_{\mathrm{bi}}+r_{\mathrm{ce}})c_{\mathrm{bce}}]^2 \ll 1$, where we assume $c_{\mathrm{bce}} \approx c_{\mathrm{bci}}$ and $r_{\mathrm{ce}} \approx r_{\mathrm{ci}}$.

III. Parameter Extraction Methodology

The InP/InGaAs HBT's characterized here were fabricated from metal organic vapor phase epitaxy (MOVPE)-grown material, with $2 \times 10\ \mu\mathrm{m}^2$ emitter area. The details of the processing and epitaxial structure have been published elsewhere [9]. The small-signal measurements were performed from 250 MHz to 36 GHz with a network analyzer, with data acquisition and analysis performed running commercial software.[1] The footprints of the transistor and test structures were designed on the ground-signal-ground (GSG) configuration. Two test structures, an "open" and a "short," were included along with the transistors to estimate the parasitics (capacitances and inductances) [3], [11]. Examples of the equivalent circuit parameters are discussed below.

A. Total Base-Collector Capacitance

In Fig. 2 we plot (5) with the measured device Z-parameters, before and after the de-embedding, $Z_{\mathrm{meas}_{ij}}$ and $Z_{\mathrm{de}_{ij}}$, respectively. From this plot, the difference between the two values is the parasitic capacitance c_{pbc} value. This value is usually extremely flat with a standard deviation of 1% or less. The discrimination between the intrinsic (c_{bci}) and extrinsic (c_{bce}) parts of the total capacitance c_{bct} will be possible only later in the optimization step, where the fitted S-parameters and the measured S-parameters are matched. So, c_{bct} will be a constraint value during the optimization.

B. Total Base Resistance

Fig. 3 shows the plot of (6), the total base resistance r_{bt}, with the measured device Z-parameters, before and after the de-embedding. This parameter mean value must also be extracted in the frequency region of 1–10 GHz. Although this value is usually very flat with a standard deviation around 2%, there is a small decrease between 8–10 GHz, which we will address with an extrinsic base contact capacitance, $c_{b,\mathrm{con}}$ shown in Fig. 1, due to the nonalloyed base metal contacts [3], [12].

The distribution between the intrinsic (r_{bi}) and extrinsic (r_{be}) parts of the base resistance r_{bt} and the evaluation of the contact capacitance will be possible only later in the optimization step. This value, r_{bt}, will be the second constraint value during the optimization. The two constraints, namely c_{bct} and r_{bt}, will together determine the distributed base impedance in the 1–8-GHz region, and the base contact capacitance $c_{b,\mathrm{con}}$ will correct this impedance at higher frequencies.

C. Collector Resistance

For our InGaAs/InP technology (7), for r_{ct}, presents a different behavior than that seen in [5] (a GaAs-based HBT

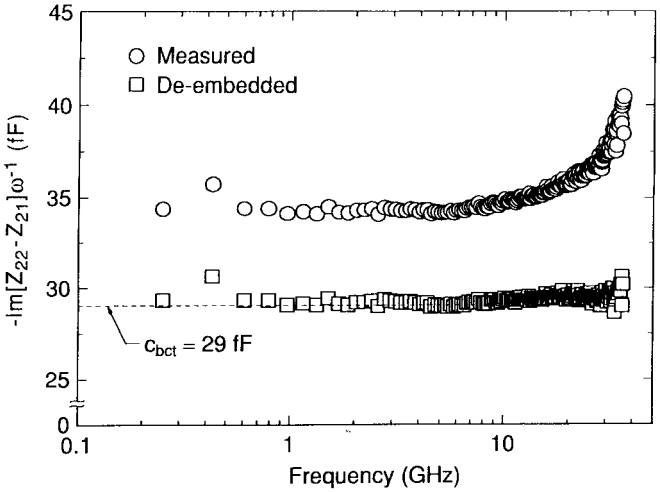

Fig. 2. Frequency dependence of the total base-collector junction capacitance, c_{bct}. The dotted line indicates the mean extracted value.

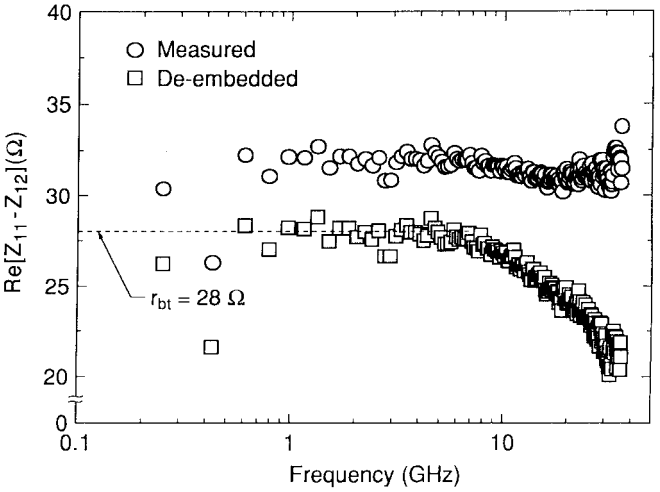

Fig. 3. Frequency dependence of the total base resistance, r_{bt}. The dotted line indicates the mean extracted value.

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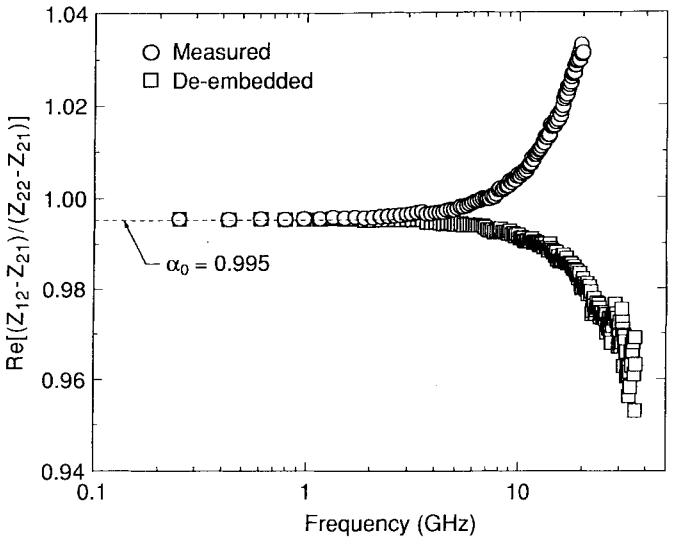


Fig. 4. Frequency dependence of the current gain magnitude, α. The dotted line indicates the low-frequency mean extracted value, presented in Fig. 1.

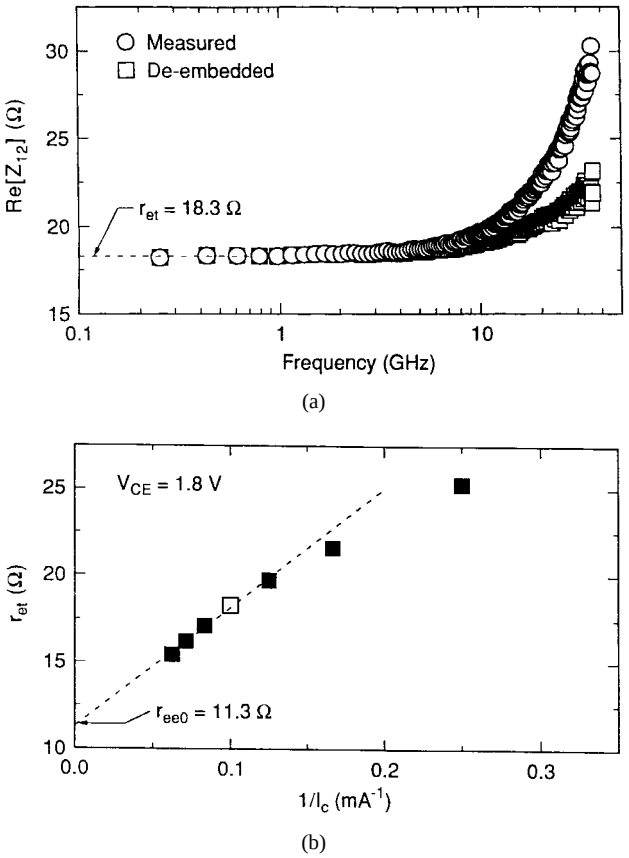


Fig. 5. (a) Frequency dependence of the total emitter resistance, $r_{\rm et}$. The dotted line indicates the mean extracted value. (b) Mean extracted values of $r_{\rm et}$ as a function of I_C^{-1}, at fixed $V_{\rm CE}$. The dotted line indicates the extrapolation to zero value, $r_{\rm ee0}$. The open square point shows a generic bias point to be simulated.

with large dimensions). First, it is extremely sensitive to the parasitic collector–emitter capacitance, $c_{\rm pce}$, that must be de-embedded in smaller devices, such as ours. Also, the second term in (7) is dominated at high frequencies by the high intrinsic base resistance, $r_{\rm bi}$, causing the total collector resistance value to become negative, with high standard deviation, and therefore, meaningless.

We choose to obtain the collector resistances from dc measurements so they could be kept constant during the optimization process. The normal measurement method [13], the stepped collector current method, is used to obtain the sum of the resistances, $r_{\rm ci} + r_{\rm ce}$. The distinction between the intrinsic and extrinsic parts, $r_{\rm ci}$ and $r_{\rm ce}$, was done utilizing the open collector method, with the emitter and collector exchanged, and assuming that this lower collector resistance result is mainly the extrinsic part due to contact resistance. Fig. 1 shows the values we found, with a standard deviation of 1 Ω.

From (8), at low frequencies this parameter will approach the base–collector junction resistance value. This would imply that the measurements have to be performed down to low frequencies (a few megahertz in our InP technology) for a precise value. Since we limit our measurements down to 250 MHz, $r_{\rm ct}$ will be useful only to obtain an order-of-magnitude estimate of the base-collector junction resistance, $r_{\rm bc}$.

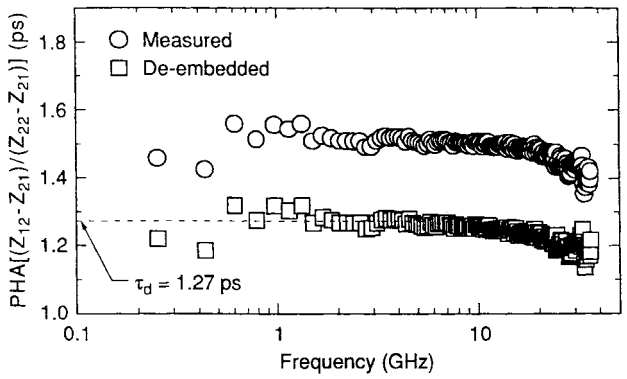
D. DC Current Gain

Fig. 4 shows the plot of (9), the dc current gain, α_0, showing that de-embedding affects it marginally. This parameter is treated as a constant during the optimization step.

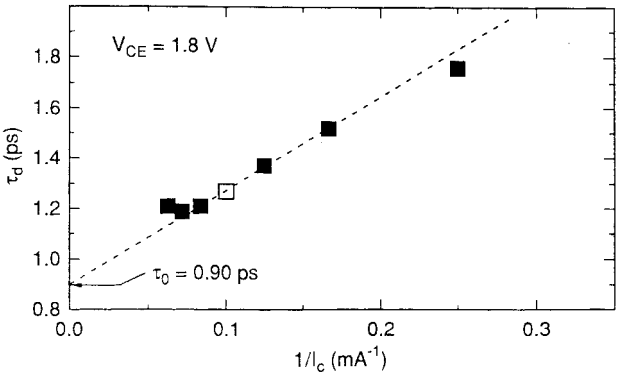
E. Total Emitter Resistance

The first two terms of (11) form the well-known low-frequency limit for the real part of Z_{12} [4], from which the total emitter resistance is usually obtained. But with the addition of an extrinsic base–collector capacitance, as in the case of InP-based HBT's, this can imply the necessity of measurements down to 10 MHz or less. So, we chose to retain a third term in the approximation, δ, as a correction. This correction can be important for HBT's with high intrinsic base resistance and low dc current gain. Fig. 5(a) shows the plot of (11), $r_{\rm et}$. It is clear that the de-embedding does not affect this value in this region. The mean value presents a standard deviation of less than 0.5%, in spite of the fact that we have only five measurement points below 1 GHz.

It is known that $r_{\rm et}$ varies inversely with the emitter current due to the dynamic emitter resistance, r_e. As $I_E \approx I_C$ for large I_C values, r_e vanishes, leaving only $r_{\rm ee}$ [4]. We therefore fixed the collector–emitter voltage, $V_{\rm CE}$, and acquired data for different collector current values. In Fig. 5(b), we plot the extracted values, $r_{\rm et}$, as function of I_C^{-1}. The extrapolated value for $I_C^{-1} = 0$ will be the extrinsic emitter resistance, $r_{\rm ee}$, plus a correction term δ. We call this sum $r_{\rm ee0}$, and use it as the first order approximation value for the extrinsic emitter resistance during the optimization step. As soon as we obtain the first values for the intrinsic base resistance, $r_{\rm bi}$, and the extrinsic base–collector capacitance, $c_{\rm bce}$, we are able to evaluate δ and correct $r_{\rm ee}$ for its new value. Usually the process converges with only two or three iterations to a stable value. In Figs. 5(b) and 1 we can see the first approximation,



(a)



(b)

Fig. 6. (a) Frequency dependence of the time delay, τ_d. The dotted line indicates the mean extracted value. (b) Mean extracted values of τ_d as a function of I_C^{-1}, at fixed $V_{\rm CE}$. The dotted line indicates the extrapolation to zero value, τ_0. The open square point shows a generic bias point to be simulated.

$r_{\rm ee0}$, and the final value, $r_{\rm ee}$. In this case, the resulting correction is small, less than 3% of the $r_{\rm ee}$ value. In other devices, grown by other epitaxy technique (viz. MOMBE) and with lower dc current gain, α_0, this correction can be as large as 18% of $r_{\rm ee}$.

Finally, the dynamic emitter resistance r_e is given by

$$r_e = r_{\rm et} - r_{\rm ee0}. \tag{12}$$

F. Time Delay

Fig. 6(a) shows the plot of expression (10), τ_d, the time delay. The de-embedding affects this parameter considerably. The standard deviation is around 2% if we restrict the extraction to the region above 1 GHz, which corresponds to the flatter section. As we can see from expression (10), τ_d has the same dependence as $r_{\rm et}$ on the emitter dynamic resistance, r_e. In Fig. 6(b) the extrapolated value of τ_d for $I_C^{-1} = 0$, called τ_0, is obtained from the linear region just before the degradation of f_T. This value corresponds to the sum of the intrinsic time delay, τ_i, and the collector charging components, $r_{\rm ci}c_{\rm bci} + r_{\rm ce}c_{\rm bct}$. At this point in the optimization, we still do not know the partition between intrinsic and extrinsic base-collector capacitances. Therefore, the τ_0 parameter value will be the third constraint in the optimization step.

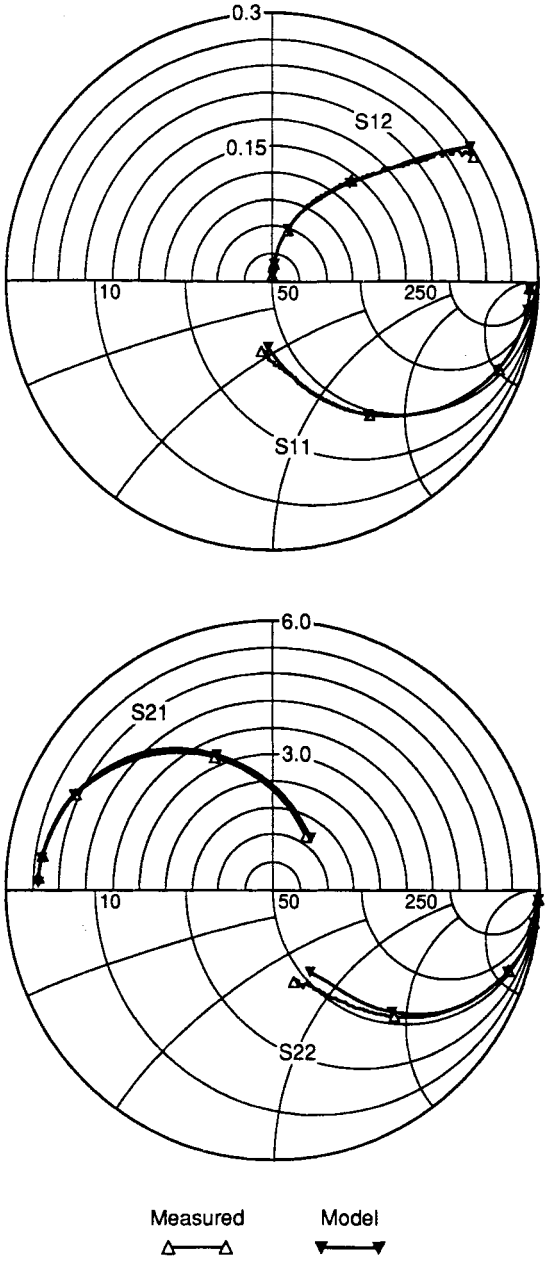


Fig. 7. Comparison between the measured and modeled S-parameters for the MOVPE grown HBT, with emitter area of 2×10 μm^2. The bias conditions and extracted parameters are shown in Fig. 1.

Now we are able now to estimate the base–emitter capacitance parameter from the expression:

$$c_{\rm be} = \frac{(\tau_d - \tau_0)}{r_e}. \tag{13}$$

G. Optimization Process

During the optimization step, the program will try to adjust the equivalent circuit (shown in Fig. 1) modeled S-parameters to the measured ones. The object is to minimize an error function, and a common problem encountered here is the convergence to a wrong minimum. To avoid this problem, we must use as few free parameters as possible, and include some constraint values. At this point of the method, the

parasitic elements $l_b, l_e, l_c, c_{\rm pbc}, c_{\rm pbe}$, and $c_{\rm pce}$, and the device parameters $r_{\rm ee0}, r_e, c_{\rm be}, r_{\rm bc0}, r_{\rm ce}, r_{\rm ci}$, and α_0 have been fixed. Furthermore, the following constraint parameters: $r_{\rm bt}, c_{\rm bct}$, and τ_0 have allowed us to reduce the free parameters to only three, namely, $r_{\rm be}, c_{\rm bci}$, and $c_{b,\rm con}$.

The base-collector junction resistance, $r_{\rm bc0}$, does not affect the results significantly and it can be fixed to a high value (order of megaohms), if compatible with the technology. After the first iteration of the optimization, (7) can be modeled for the value of $r_{\rm bc}$, and adjusted to obtain the initial sharp increase at low frequencies (in this case, 1 GHz).

Now we repeat the iterations to correct the initial extrinsic emitter resistance, $r_{\rm ee0}$. This process must be done carefully as this parameter affects the results much more significantly. But in this case we have one of the most precise values from the extraction method. The effect of the small correction, δ, can be seen clearly in the low frequency behavior of S_{21}, shown in Fig. 7.

After a few iterations, the final constant values are obtained and the optimization is free to quickly converge to the final result for all device parameters. Fig. 7 shows the modeled and measured S-parameters of the HBT with the parameter value results at the bottom of Fig. 1.

Due to the effect of parasitic capacitance fluctuations, around 10% in our measurements, we estimate that the accuracy of base–collector capacitances is within ± 0.5 fF, of the base resistances is $\pm 1\ \Omega$ and the intrinsic delay time is within ± 0.03 ps. The parasitic inductances had a smaller effect on the results, due to their small deviations. But some caution must be taken with respect to the parasitic base inductance value, l_b. This parameter is an element in the imaginary part of the total base impedance and influences the distribution between intrinsic and extrinsic base-collector junction capacitances.

IV. Conclusion

In summary, we have presented a self-consistent method for direct calculation of the parameters of the T-model equivalent circuit from S-parameters of an InGaAs/InP HBT. With just two test structures on the same wafer, we are able to derive resistances, capacitances, transit times, and their bias dependence (if needed) and investigate which parameters most affect the transistor performance. The analytical expressions derived for the equivalent circuit model allow one to analyze the technology aspects and further parasitic reduction.

The approach presented here can be incorporated in the analysis of any HBT-based technology and provide insight in the physics of the device.

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She joined AT&T Bell Laboratories, Murray Hill, NJ, in 1985, where she initiated the GaAs-based heterojunction bipolar transistor (HBT) circuit technology for transmission systems applications. She developed novel device structures for the HBT, including quantum support such as the resonant tunneling bipolar transistor. One of these structures was for a self-aligned technology for ease in manufacturing. From 1990 to 1995, she was with the Photonics Devices Research Department, Holmdel, NJ, where she worked on different circuit architectures for the monolithic optoelectronic integration of InP-based HBT's for wavelength receiver system applications. In January 1996, she joined the Broadband Access Research Department in the newly formed AT&T Laboratories-Research, where she has been working in electronic component for novel local access architectures. Her publications include over 40 papers and two patents in the area of compound semiconductor devices and circuit applications.

Dr. Lunardi was Associate Editor of the IEEE Electron Device Letters from 1990 to 1992 and has served on technical program committees of several conferences. She is a member of the IEEE Electron Devices Society and the American Physical Society.

S. Chandrasekhar (M'90) was born in Tiruchirapalli, Tamil Nadu, India, on January 26, 1952. He received the B.Sc., M.Sc., and Ph.D. degrees in physics from the University of Bombay, Bombay, India, in 1973, 1975, and 1985, respectively.

He joined the Tata Institute of Fundamental Research, Bombay, as a Research Scholar in 1975 and became a Research Associate in 1979. He had been engaged in research on Si–SiO_2 interface studies, CMOS integrated circuits, ion implantation, charge coupled devices, and laser recrystallization. In 1986, he joined AT&T Bell Laboratories (now Bell Labs, Lucent Technology), Crawford Hill Laboratory, Holmdel, NJ, as a postdoctoral member of Technical Staff. Since then, he has been working on III–V compound semiconductor devices for optoelectronic applications, primarily waveguides, photodetectors, heterojunction phototransistors, and bipolar transistors (HBT's). He returned to T.I.F.R. in September 1988, but rejoined AT&T's Crawford Hill Lab in April 1989 as a consultant. He became a permanent member, Technical Staff, in May 1992. He has been and is currently engaged in high-speed optoelectronic integrated circuits (OEIC's), using HBT's, for long wavelength optical communications. He holds one U.S. patent.

Dr. Chandrasekhar is a member of the IEEE Electron Devices Society and the IEEE Lasers and Electro-Optics Society. He has been a member of the technical program committee of the IEDM, the DRC, and the OFC conferences.

Y. Miyamoto, photograph and biography not available at the time of publication.